Alpha Bridge SFP AQSFP28-100G-LR4-CBD Datasheet

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Features

- Hot pluggable QSFP28 MSA form factor
- Compliant to IEEE 802.3ba 100GBASE-LR4
- Supports 103.1Gb/s aggregate bit rate
- Up to 10km reach for G.652 SMF
- Single +3.3V power supply
- Operating case temperature: 0~70℃
- Transmitter: cooled 4x25Gb/s LAN WDM DFB TOSA (1295.56, 1300.05, 1304.58, 1309.14nm)
- Receiver: 4x25Gb/s PIN ROSA
- 4x25G electrical interface (OIF CEI-28G-VSR)
- Maximum power consumption 4.0W
- Duplex LC receptacle
- RoHS-6 compliant

Application

- 100GBASE-LR4 Ethernet Links
- Infiniband QDR and DDR interconnects
- Datacenter and Enterprise networking

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	Ts	-40	85	℃	
Power Supply Voltage	Vcc	-0.5	3.6	V	
Relative Humidity(non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	THd	5.5		dBm	
Operating Case Temperature	*Top*	0	70	℃	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Typ.
Case operating Temperature	Top	0	70	°C	
Supply Voltage	Vcc	3.135	3.465	V	3.3
Data Rate, each Lane				Gb/s	25.78125

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Data Rate Accuracy		-100	100	ppm	
Control Input Voltage High		2	Vcc	V	
Control Input Voltage Low		0	0.8	V	
Link Distance with G.652	*D*	0.002	10	km	

Transmitter Electro-optical Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Units	Note
Power consumption				4	W	
Supply Current	Icc			757	mA	
Overload Differential Voltage pk-pk	TP1a	900			mA	
Common Mode Voltage (Vcm)	TP1	-350		2850	mA	1
Differential Termination Resistance Mismatch	TP1			10	%	At 1 Hz
Differential Return Loss (SDD11)	TP1	See CEI-28G- VSR Equation 13-19			dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC11, SCD11)	TP1	See CEI-28G-VSR Equation 13-20			dB	
Stressed Input Test	TP1a	See CEI-28G-VSR Section 13.3.11.2.1				
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	PT			10.5	dBm	
Average Launch Power,each Lane	PAVG	-4.3		4.5	dBm	
OMA, each Lane	POMA	-1.3		4.5	dBm	2
Difference in Launch between any Two Lanes (OMA)	Ptx, diff			5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP),each Lane		-2.3				
TDP, each Lane	TDP		.2		dB	
Extinction Ratio	ER	4			dB	
$RIN_{20}OMA$	RIN			-130	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	RT			-12	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					3

Notes:

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
3. Hit ratio $5x10^{-5}$.

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Receiver Electro-optical Characteristics

Parameter	Test Point	Min.	Typ.	Max.	Units	Note
Differential Voltage, pk-pk	TP4			900	mV	
Common Mode Voltage (Vcm)	TP4	-350		2850	mV	1
Common Mode Noise, RMS	TP4			17.5	mV	
Differential Termination Resistance Mismatch	TP4			10	%	At 1MHz
Differential Return Loss (SDD22)	TP4	See CEI- 28G-VSR Equation 13-19			dB	
Common Mode to Differential conversion and Differential to Common Mode conversion (SDC22, SCD22)	TP4	See CEI- 28G-VSR Equation 13-21			dB	
Common Mode Return Loss, (SCC22)	TP4			-2	dB	2
Transition Time, 20 to 80%	TP4	9.5			ps	
Vertical Eye Closure (VEC)	TP4			5.5	dB	
Eye Width at 10-15 probability (EW15)	TP4	0.57			UI	
Eye Height at 10-15 probability (EH15)	TP4	228			mV	
Damage Threshold, each Lane	THd	5.5			dBm	3
Average Receive Power, each Lane		-10.6		4.5	dBm	
Receive Power (OMA), each Lane				3	dBm	
Receiver Sensitivity (OMA), each lane	SEN			-9.2	dBm	BER=5x10-5
Stressed Receiver Sensitivity (OMA), each Lane				-5.2	dBm	4
Receiver Reflectance	RR			-12	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-13		
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3dB upper Cutoff Frequency, each Lane	Fc			31	GHz	
Conditions of Stress Receiver Sensitivity Test (Note 5)						
Vertical Eye Closure Penalty, each Lane			1.8		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Notes:

1. Vcm is generated by the host. Specification includes effects of ground offset voltage.
2. From 250MHz to 30GHz.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical inputsignal having this power level on one lane. The receiver does not have to operate correctly at this input power.

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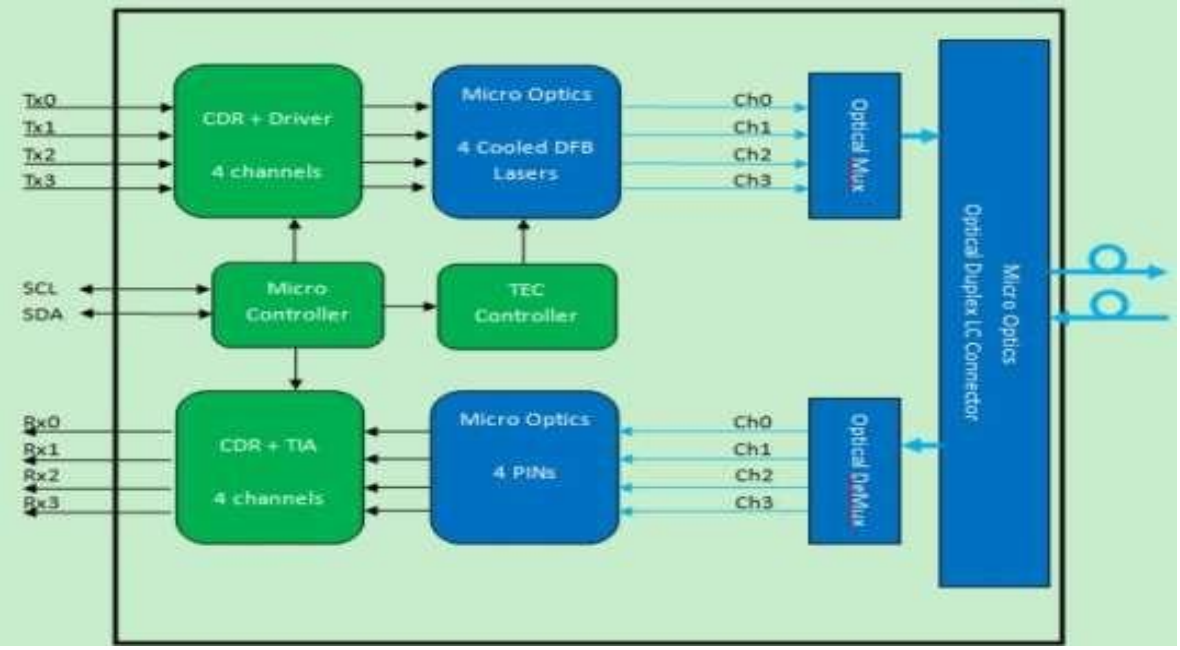
4. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$.
5. Vertical eye closure penalty, stressed eye J2 jitter, and stressed eye J9 jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Block Diagram of Transceiver



This product is a 100Gb/s transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE 802.3ba standard. The module converts 4 input channels of 25Gb/s electrical datato 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14 nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high-performance cooled LAN WDMDFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant to optical interface with 100GBASE-LR4 requirements specified inIEEE 802.3ba Clause 88.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface accordingto the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently,DFB laser driver IC converts each one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled DFB lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE 802.3ba 100GBASE- LR4 requirements. These 4-lane optical signals will be optically multiplexed into a single fiber by a 4-to-1 opticalWDM MUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or 2-wire serial interface.

The receiver receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by a 1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value isreported through the 2-wire serial interface. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

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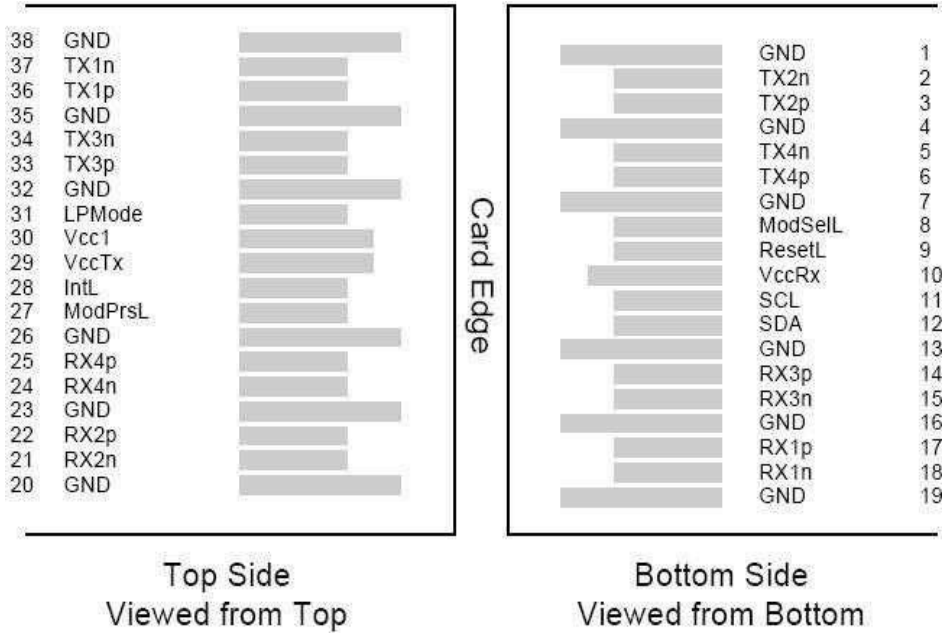
A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 lowspeed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface andenable the host to access the QSFP28 memory map.
The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by postingan IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset. Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order toprotect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normallypulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a "Low" state. Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an opencollector output and must be pulled to the Host Vcc voltage on the Host board.

Pin Assignment (MSA compliant connector)



Pin Descriptions

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter inverted Data Input	

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6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSeIL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GNC	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data output	
15	CML-O	Rx3n	Receiver Inverted Data output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data output	
22	CML-O	Rx2p	Receiver Non-Inverted Data output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply transmitter	2
30		Vcc1	+3.3V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 andVcc Tx may be internally connected within the module in

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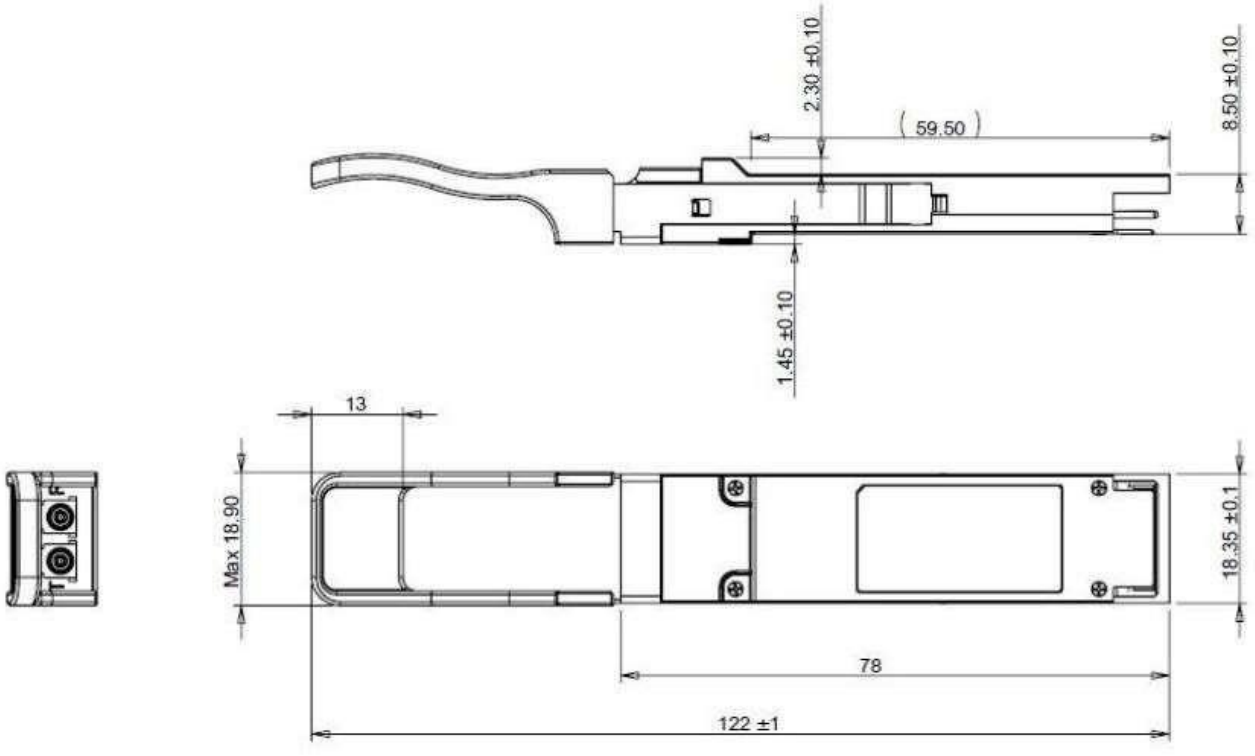
any combination. The connector pins are each ratedfor a maximum current of 1000mA.

Dimensions



Note: Dimensions are in mm, All Dimensions are 0.2mm unless otherwise specified

Ordering information:

Model Number	Part Number	Voltage	Temperature
AQSFP28-100G-LR4-CBD	OPCW-S40-13-CR	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.

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